



Memory Technology in HP Z Workstations



DDR3

DDR3 is the latest memory technology available for main memory on high volume mobile, desktops, workstations, and server computers. DDR stands for Double Data Rate which transfers data on both the rising and falling edges of the clock signal. The key benefit over its predecessor, DDR2, is its ability to transfer data at twice the rate which enables higher bandwidth. DDR3 also enables significant power savings over DDR2. It is not forward or backwards compatible with any other type of RAM.

DDR3 Interface

The DDR3 memory interface connects the Dual In-line Memory Module (DIMMs) to the CPU and consists of address/command and data bus groups. The data bus group is comprised of 64 bits on non-ECC systems and 72 bits on processors and systems that support ECC memory.

Memory Module Makeup

A DDR3 DIMM consists of a number of distinct parts or components such as: the raw card or Printed Circuit Board (PCB), DRAM chips, buffer register in the case of RDIMMs and LRDIMMs, and various discrete components. The DRAM chips used define the principal characteristics of a DIMM, along with the number of ranks that participate in the resulting capacity of a DIMM.

DRAM Characteristics

Dynamic Random Access Memory (DRAM) chips come in different capacities. Today, 2 Gigabit (Gb) DRAMs are the most common and considered to be the best value. 4Gb DRAMs are available, but carry a price premium. 8Gb DRAMs are expected to be available in the first half of 2013.

DRAM chips can support 4, 8, or 16 data bits of width per chip. The width of the DRAM is designated by $x\#$, for example a 4 bit width DRAM is $x4$. The size and the width of a DRAM provide flexibility in creating DIMMs of different organizations to create the optimal DIMM at each capacity for each type. Since some DRAMs are single, dual or quad dies, the number of chips on a DIMM is an unreliable way to guess the type of DRAM used.

DRAMs can operate at ultra-low voltage (1.25V), low voltage (1.35V), and normal voltage (1.5V). The higher voltages enable greater memory speed and increased margin of the memory subsystem.

ECC Protection

Error Correction Code (ECC) provides protection against some data bit corruption events, either in the DRAM chips on the DIMM, or on the memory bus and in the platform's memory controller. On ECC DIMMs, 8 additional data bits are implemented, giving a data bus width of 72 bits instead of 64 bits on non-ECC DIMMs.

Additional DRAM chips provide the additional memory space needed for the ECC protection. For each data transfer to the DIMM during a write event, an ECC code is calculated by the memory controller and stored along with the data to be written. On subsequent reads, the memory controller checks the ECC code and can determine if single-bit or multiple-bit errors occurred. It will correct single-bit errors automatically, thereby avoiding propagation of corrupted data to the system. Multi-bit errors cannot be corrected on platforms with independent memory channels, as in the case on most current Workstation systems, as opposed to channels in lockstep mode. However, multi-bit errors can be detected and, on HP Workstations, will immediately trigger a Machine Check event which will halt the operating system, thus preventing the propagation of corrupted data.

Non-ECC DIMMs have no extra data bits and so do not provide protection against incorrect data bit values. Non-ECC memory does not detect or correct single-bit or multi-bit errors. This can lead to system crashes, or data corruption without alerting the user. Data corruption can take many forms, such as: applications processing incorrect data, delivering incorrect results, applications crashes, or file corruption. File corruption can lead to an inability to reopen a file, the need to reinstall either an application or the operating system. ECC improves protection against corruption of data in memory and should be used in mission critical applications or high-reliability, 24 x 7 x 365 environments.

Ranks

A Rank is defined to be a group of DRAM chips with matching characteristics such that the sum of the DRAM widths is either 64 bits (non-ECC) or 72 bits (ECC). Two examples are:

- 1 Rank = 8 x [x8 DRAM] = 64 bits
- 1 Rank = 18 x [x4 DRAM] = 72 bits

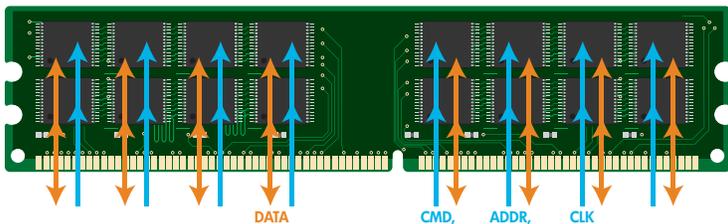
To increase capacity on a DIMM, additional ranks can be added. A memory rank is a set of DRAMs connected by a chip select line. This allows multiple DRAMs to be selected at the same time, so that each can provide their share (4, 8, or 16 data bits) of the 64 or 72 bit bus width.

DDR3 Memory Module Types

There are three types of DIMMs supported in HP Workstations: unbuffered, registered, and load reduced. Note that these DIMM types cannot be intermixed in a system.

FIGURE 1

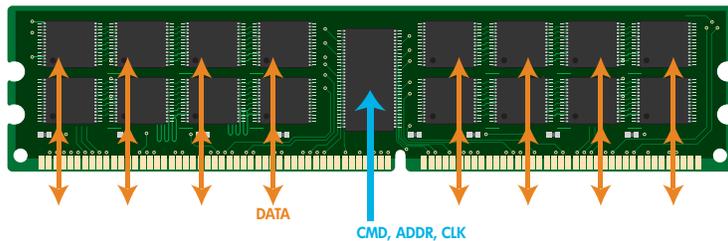
Unbuffered DIMMs (UDIMM)



Unbuffered DIMMs (UDIMM) are high volume DIMMs used in most consumer and entry enterprise applications. As the name implies, none of the signals are buffered. The data and command/address signals go directly into the DRAMs, as shown in the figure below. There are two types of UDIMMs: non-ECC and ECC. Non-ECC UDIMMs can support x8 and x16 DRAMs. ECC UDIMMs can only support x8 DRAMs.

FIGURE 2

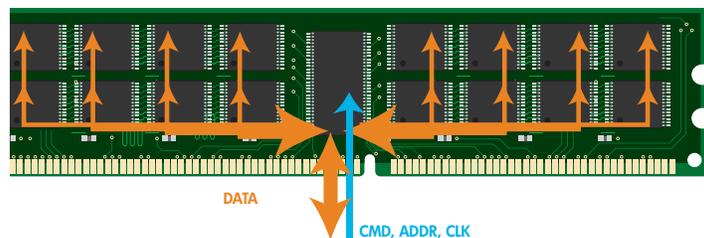
Registered DIMMs (RDIMM)



Registered DIMMs (RDIMM) use registers to buffer the command and address signals, as shown in the figure below. The data bits are not buffered. All registered DIMMs support ECC as well as parity protection on the command and address signals. There is added clock latency when compared to a UDIMM. RDIMMs should be used for higher reliability and for cost savings on higher capacities. Both x8 and x4 DRAMs can be supported, allowing larger memory capacities than UDIMMs by essentially doubling the number of DRAM chips which can be installed on a DIMM. RDIMMs can also present a large price advantage compared to large capacity UDIMMs as new DRAM chip density carries a price premium over the current high volume DRAM density.

FIGURE 3

Load Reduced DIMMs (LR DIMM)



Load Reduced DIMMs (LR DIMM) are a new technology that use registers to buffer command, address, and data signals, as shown in the figure below. ECC and parity are supported on LR DIMMs. LR DIMMs were created to reduce the electrical data load on the system's memory bus to a single load. This buffering architecture removes some of the speed and signal integrity limitations experienced with RDIMMs, and enables added capacity at increased speeds. The reduced load enables the use of quad and octal ranks DIMM architecture. Octal rank DIMMs double the memory capacity over a quad rank RDIMM. There are also power savings per Gigabyte and added clock latency when compared to an RDIMM. Only x4 DRAMs are supported. LR DIMMs should be used if high capacity memory using today's technology is desired.

TABLE 1

Current available DIMM type support table

	Unbuffered Non ECC	Unbuffered ECC	Registered	Load Reduced
Single rank	X	X	X	
Dual rank	X	X	X	
Quad rank			X	X
Octal rank				X
16 bit width DRAMs (x16)	X			
8 bit width DRAMs (x8)	X	X	X	
4 bit width DRAMs (x4)			X	X
ECC data protection on data		X	X	X
Parity protection on Command/Address			X	X
Buffered Command/Address/Clock			X	X
Buffered data				X

Memory Module Capacity Calculation

As mentioned previously, capacity is calculated using DRAM characteristics, specifically technology, width, and the total number of ranks. ECC should be considered in calculating the amount of DRAMs needed, but the ECC DRAM(s) are only used to hold the ECC values calculated and should not be counted as part of the actual data payload which defines the DIMM capacity.

To calculate the capacity of a DIMM, the type of DRAMs used must be understood. The width of the DRAM should be used to find the number of DRAMs needed to make up the data bus. The capacity per rank can then be calculated by multiplying the number of DRAMs by the size of the DRAM, and further divided by 8 to convert bits into bytes. The total DIMM capacity is finally calculated by multiplying the rank capacity and the number of ranks on the DIMM. On the next page are two examples:

4GB Unbuffered, Dual-Rank, ECC DIMM

Rank width = [9 DRAM] x [x8 width] = 72 bits

Rank Capacity = [8 Payload DRAM] x [2 Gb technology]/[8 bits] = 2 GB

DIMM Capacity = [2 Ranks] x [2 GB per Rank] = 4 GB

32GB Registered, Quad-Rank, ECC DIMM

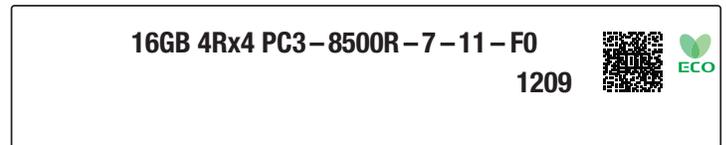
Rank width = [18 DRAM] x [x4 width] = 72 bits

Rank Capacity = [16 Payload DRAM] x [4 Gb technology]/8 bits = 8 GB

DIMM Capacity = [4 Ranks] x [8 GB per Rank] = 32 GB

Using the above calculation, the max capacity available today, with 4 Gb based RDIMMs, can be calculated to 32 Gigabyte (GB). 8 Gb DRAMs are expected to be available in the first half of 2013, for a the max capacity per RDIMM 64 GB but at a significant price premium.

Label Decoder



The following should be used to understand key attributes about the type of memory that is loaded in a system. When looking at the DIMM label, you should see the following format:

aaGB bRxc PC3-dddddde-f-g-h

a = total capacity of the DIMM

b = number of ranks of memory

c = bit width of the DRAM installed

(e.g. x4, x8, x16)

PC3 = Indicates that the is a DDR3 module and what voltage the DIMM operates at

PC3 = operates at 1.5V

PC3L = operates at 1.35V

d = DIMM bandwidth.

To understand the speed that the memory is running at, divide the bandwidth by eight and then round up to the closest memory speed. For example, 10600 MB/s bandwidth converts to 1333MHz memory speed.

e = module type.

U = Unbuffered

E = ECC unbuffered

R = Registered

P = Parity Registered

L = LR DIMM

f = CAS Latency, minimum RCD, and minimum RP in clocks at the maximum frequency

g = SPD revision encoding

h = Reference design and reference number

Additional Resources

- Tezzaron Semiconductor: Soft Errors in Electronic Memory: White Paper 2004
http://www.tezzaron.com/about/papers/soft_errors_1_1_secure.pdf
- University of Toronto Study: DRAM Errors in the Wild: A large-Scale Field Study; A cooperative study with Google of DRAM failures in actual use.
<http://www.cs.utoronto.ca/~bianca/papers/sigmetrics09.pdf>
- Cycles, Cells and Platters: An Empirical Analysis of Hardware Failures on a Million Consumer PCs
<http://dl.acm.org/citation.cfm?id=1966477>
- HP Workstation Individual Platform Memory Configurations and Optimization White Papers

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4AA4-0295ENW, April 2012